CBCS SCHEME

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17EC34

Third Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. Define the following:
i) Combinational circuit
ii) Sequential circuit
iii) Canonical SOP
iv) Canonical POS
v) Prime Implicant
vi) Essential prime implicant. **(08 Marks)**

b. Express the following equations into decimal notations:
i) $H = f(A, B, C) = A'BC + A'BC + ABC$
ii) $T = f(a, b, c) = (a + b' + c)(a + b' + c')(a' + b' + c)$ **(08 Marks)**

c. Write mirror image version 5-variable K-map. **(04 Marks)**

OR

2 a. Obtain minimal expression using k-map for the following incompletely specified function $F(a, b, c, d) = \sum m(0, 1, 4, 6, 7, 9, 15) + \sum d(3, 5, 11, 13)$ and draw circuit diagram using gates. **(10 Marks)**

b. Simplify the following using Quine-Mcclusky method
$s = f(w, x, y, z) = \sum(1, 3, 13, 15) + \sum d(8, 9, 10, 11)$ **(10 Marks)**

Module-2

3 a. Explain the analysis and design procedure for combinational circuit with example. **(10 Marks)**

b. Implement full substractor using 3:8 decoder and write truth table. **(10 Marks)**

OR

4 a. Design full adder using i) 8:1 MUX ii) 4:1 MUX. **(10 Marks)**

b. Design 4 to 16 decoder using 3 to 8 decoder. **(05 Marks)**

c. Explain look ahead carry adder and give its advantages and disadvantages. **(05 Marks)**

Module-3

5 a. What is flipflop? Discuss working principle of SR flipflop with its TT and write characteristics equations. **(10 Marks)**

b. Sketch timing diagram for JK flipflop and D-flipflop. **(05 Marks)**

c. Explain the operation of a switch debouncer built using SR-latch with the help of waveforms. **(05 Marks)**

OR

6 a. Explain the working of a master-slave JK flip-flop with timing diagram. Show how race around condition is eliminated. **(10 Marks)**

b. Explain setup time, hold time and propagation delay for timing considerations. **(05 Marks)**

c. Write characteristics equation for D and T flip-flop. **(05 Marks)**

Module-4

7 a. Explain with diagram, operation and waveforms Serial In Serial Out (SISO) shift left mode register. **(10 Marks)**

b. Design BCD ripple counter using JK flip-flop. **(10 Marks)**

OR

8 a. Design an synchronous mod 5 counter using JK flip-flop and draw its timing diagram. **(10 Marks)**

b. Explain ring counter with timing sequence. **(05 Marks)**

c. Write a note on Johnson counter. **(05 Marks)**

Module-5

9 a. Draw and explain the block diagram of Moore and Mealy model with example and also compare both. **(10 Marks)**

b. Define, present state, next state, state diagram state table and state assignment. **(05 Marks)**

c. Draw and explain Moore JK-flipflop state diagram. **(05 Marks)**

OR

10 a. Analyze the synchronous sequential circuit show below in Fig.Q.10(a).

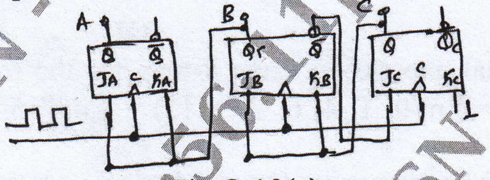

Fig.Q.10(a)

(12 Marks)

b. Design a synchronous counter using JK flipflops to count the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2. Use state diagram and state table. **(08 Marks)**

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